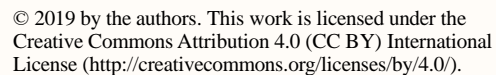
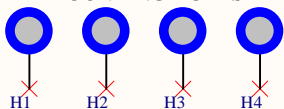


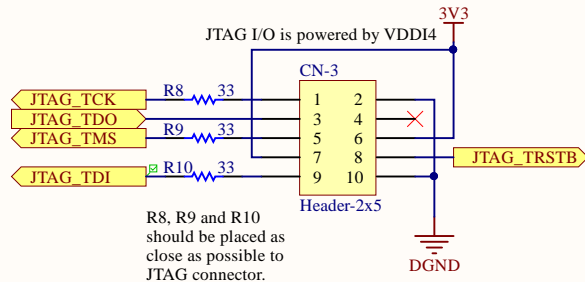
U\_Connectors  
Connectors.SchDoc

**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain

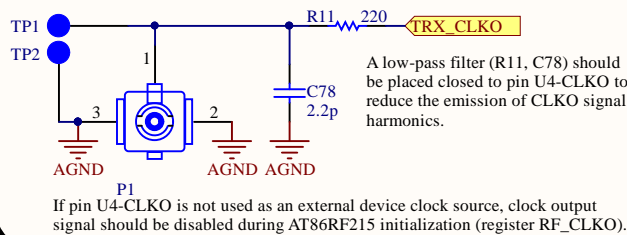


# CONNECTORS

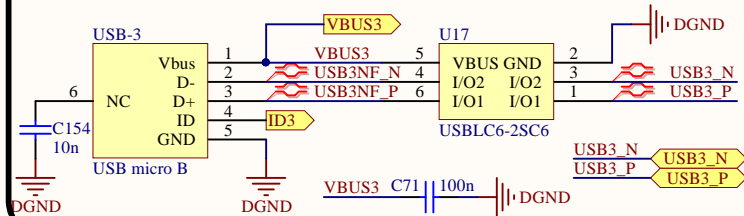
## MICROSEMI FLASHPRO JTAG CONNECTOR



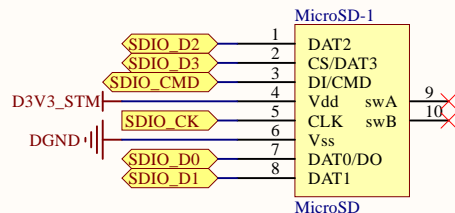
## TRANSCEIVER CLOCK OUTPUT SIGNAL



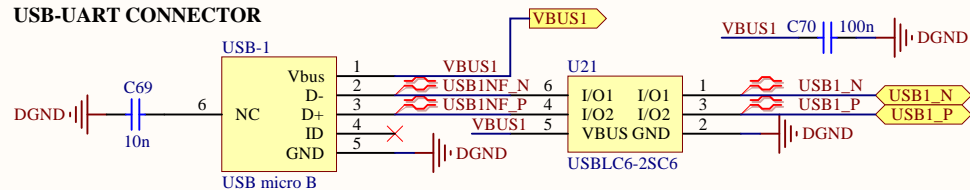
## MONITORING MCU USB



## MONITORING MCU MICRO SD



## USB-UART CONNECTOR

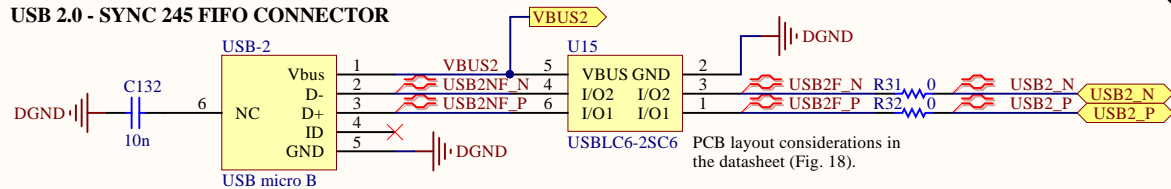


The USB DP/DM differential impedance must be 90 ohm. On a 4 layer board with 0.195 mm between outer and inner layers and with substrate dielectric 4.3:

- Trace Thickness: 17.5 um
- Trace Width 0.27 mm
- Trace spacing: 0.15 mm

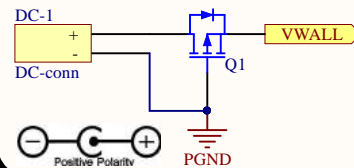
Result: Zdiff: 90.126 ohm

## USB 2.0 - SYNC 245 FIFO CONNECTOR



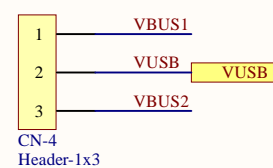
## AC ADAPTER

Supply Range: 4.2-10V



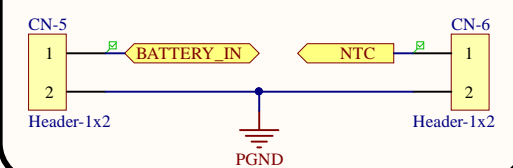
## USB POWER PORT SELECTOR

USB Supply Range: 4.2-6V

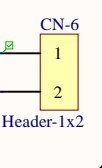


## BATTERY CONNECTOR

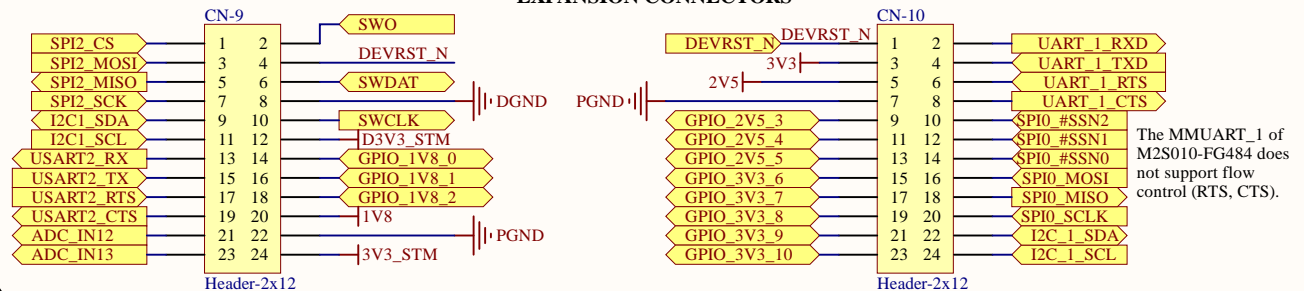
Battery Range: 3.3-4.2V



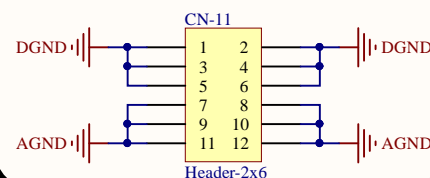
## NTC CONNECTOR



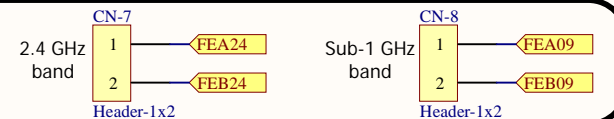
## EXPANSION CONNECTORS



## DGND & AGND PINS



## RF FRONTEND CONTROL



The MMUART\_1 of M2S010-FG484 does not support flow control (RTS, CTS).

Title: **CONNECTORS**Engineers: *Ramiro Utrilla and José Martín*

Date: 22/10/2019 Time: 11:31:30

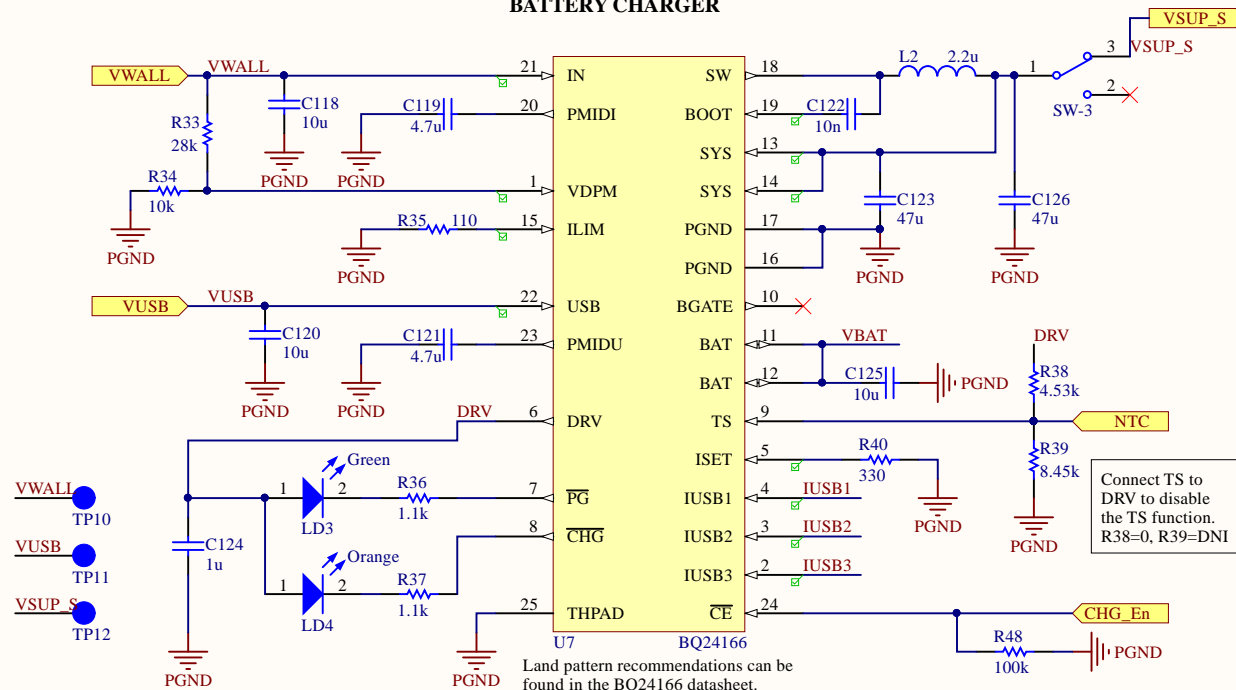
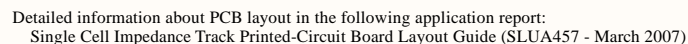
File: D:\Repositorio\migou-platform\MIGOU\Schematics\Connectors.SchDoc

Revision: v1r0

Sheet: 2 of 14

**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain





OVERVOLTAGE and overcurrent protection.  
Battery short circuit protection.

IN port:

Maximum current:	2.5 A
Operating voltage range:	4.2 - 10 V

USB port:

Maximum current:	1 A
Operating voltage range:	4.2 - 6 V

BAT port:

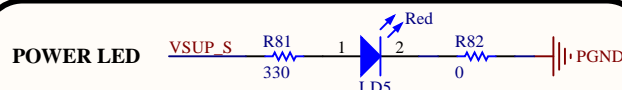
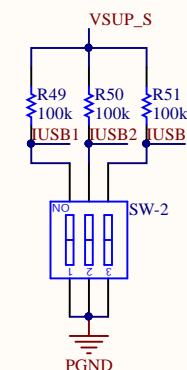
Max. chg/dischg current:	2.5 A
--------------------------	-------

Vin\_dpm= 4.56V with R33 = 28 kohm  
 I\_INlim = 2.4 A with R35 = 110 ohm  
 I\_USBlim = 0.5 A with IUSB1 = 1  
   IUSB2 = 0  
   IUSB3 = 0  
 I\_charge = 1.5A with R40 = 330 ohm  
 NTC: NXFT15XV103FA2B150 => R38 = 4.53k and R39 = 8.45k

The BQ24166 is a switch mode single cell Li-Ion/Li-Polymer battery charger with power path management. It has dual inputs which allow operation from either a USB port or an AC adapter.

SYS output powers the external system load connected to the battery. This output is active whenever a source is connected to IN, USB or BAT.

USB Input Current Limit			
IUSB3	IUSB2	IUSB1	Current Limit
0	0	0	100 mA
0	0	1	500 mA
0	1	0	1.5 A
0	1	1	Hi-Z Mode
1	0	0	150 mA
1	0	1	900 mA
1	1	0	800 mA
1	1	1	Hi-Z Mode



Title: **BATTERY AND POWER PATH MAN.**

Engineers: *Ramiro Utrilla and José Martín*Revision: *v1r0*

Date: 22/10/2019 Time: 11:31:31

Time: 11:31:31

Sheet: 3 of 14

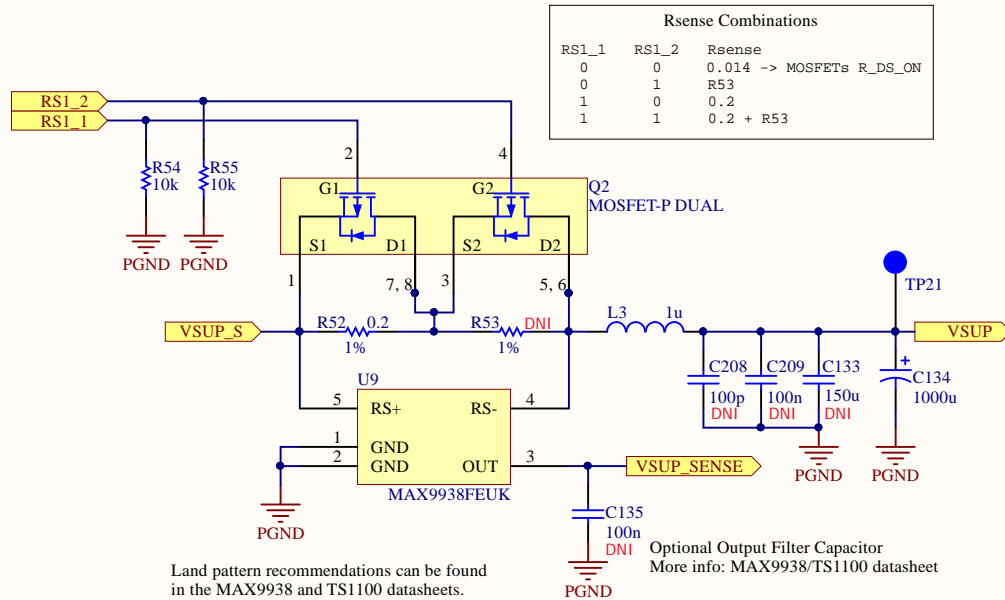
File: D:\Repositorio\migou-platform\MIGOU\Schematics\BatteryChargerFuelGauge.SchDoc

**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain



# CURRENT MONITORING

## VSUP CURRENT MONITORING



### SPECIFICATIONS:

VSUP_S Range:	3.5 - 4.2 V
Current Sensing Range:	300 uA - 300 mA
MAX9938 Gain:	50 V/V
Vsense for the full-scale:	60 mV (for gain of 50 V/V)
R_DS_ON @ V_GS = 3.3V	0.0070 Ohm

### DESIGN:

Rsense (Vsense\_fs/Iload\_max): 0.2 Ohm

P\_max = 60 mV x 300 mA = 18 mW

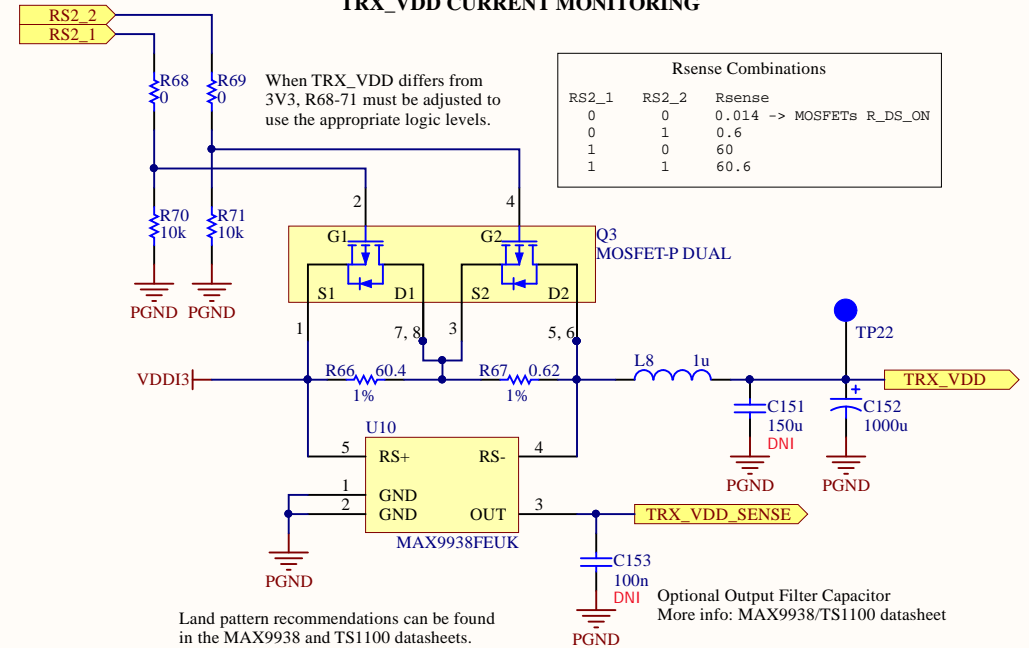
### When:

Iload\_max=300 mA => Vsense = 60 mV => Vout\_max = 3 V  
Iload\_min=300 uA => Vsense = 60 uV => Vout\_min = 3 mV

### ADC CHARACTERISTICS:

Resolution:	12-bit
Input Range:	0 - 3.6 V
Min. Voltage Step:	1 mV
Min. Current Step:	100uA

## TRX\_VDD CURRENT MONITORING



### SPECIFICATIONS:

TRX_VDD possible values:	1.8 / 2.5 / 3.3 V
Current Sensing Range:	1 uA - 100 mA
- First half (with R66):	1 uA - 1 mA
- Second half (with R67):	100 uA - 100 mA
MAX9938 Gain:	50 V/V
Vsense_max:	60 mV (for gain of 50 V/V)
R_DS_ON @ V_GS = 4.5V	0.0070 Ohm

### DESIGN:

Rsense (Vsense\_fs/Iload\_max):

- First half:	60 Ohm
- Second half:	0.6 Ohm

P\_max = 60 mV x 100 mA = 6 mW

### Using Rsense=60 Ohm, when:

Iload\_max=1 mA => Vsense = 60 mV => Vout\_max = 3 V  
Iload\_min=1 uA => Vsense = 60 uV => Vout\_min = 3 mV

### Using Rsense=0.6 Ohm, when:

Iload\_max=100 mA => Vsense = 60 mV => Vout\_max = 3 V  
Iload\_min=100 uA => Vsense = 60 uV => Vout\_min = 3 mV

### ADC CHARACTERISTICS:

Resolution:	12-bit
Input Range:	0 - 3.6 V
Min. Voltage Step:	1 mV
Min. Current Step:	- With Rsense=60 Ohm: 333nA - With Rsense=0.6 Ohm: 33uA

Title: **CURRENT MONITORING**

Engineers: Ramiro Utrilla and José Martín

Revision: v1r0

Date: 22/10/2019 Time: 11:31:33

Sheet: 4 of 14

File: D:\Repositorio\migou-platform\MIGOU\Schematics\CurrentMonitoring.SchDoc

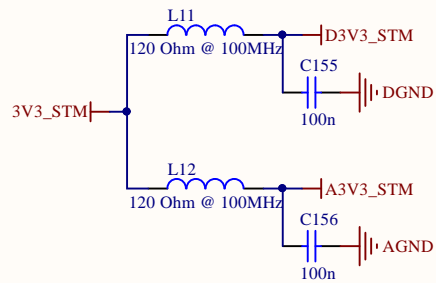
**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain



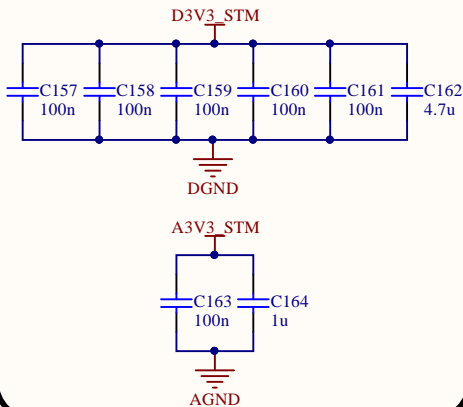


# MONITORING MCU

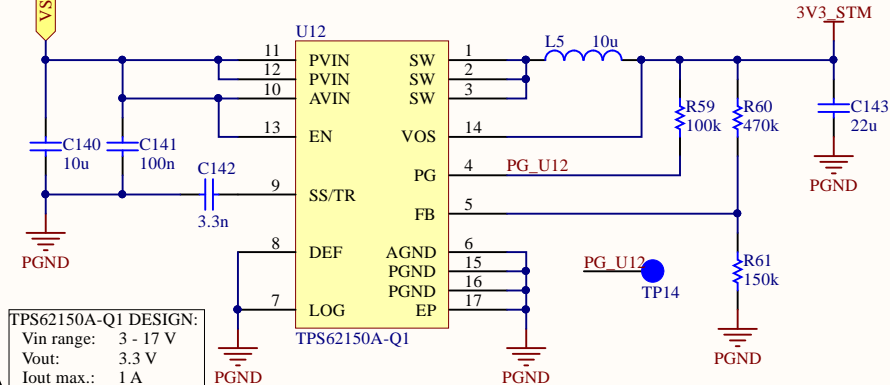
## POWER FILTERING



## POWER SUPPLY DECOUPLING

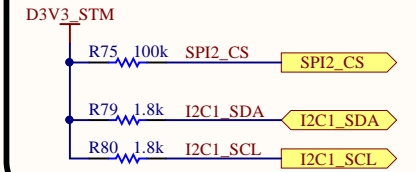


## MONITORING MCU 3.3V / 1A REGULATOR

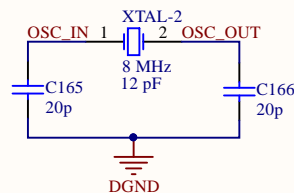


TPS62150A-Q1 DESIGN:  
Vin range: 3 - 17 V  
Vout: 3.3 V  
Iout max.: 1 A

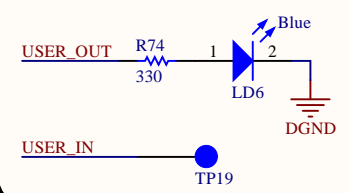
## SPI / I2C



## HIGH-SPEED EXT. CRYSTAL



## USER GPIOs



Title: **MONITORING MCU**

Engineers: Ramiro Utrilla and José Martín

Revision: v1r0

Date: 22/10/2019 Time: 11:31:35

Sheet: 6 of 14

File: D:\Repositorio\migou-platform\MIGOU\Schematics\MonitoringMCU.SchDoc

**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain



# SmartFusion2

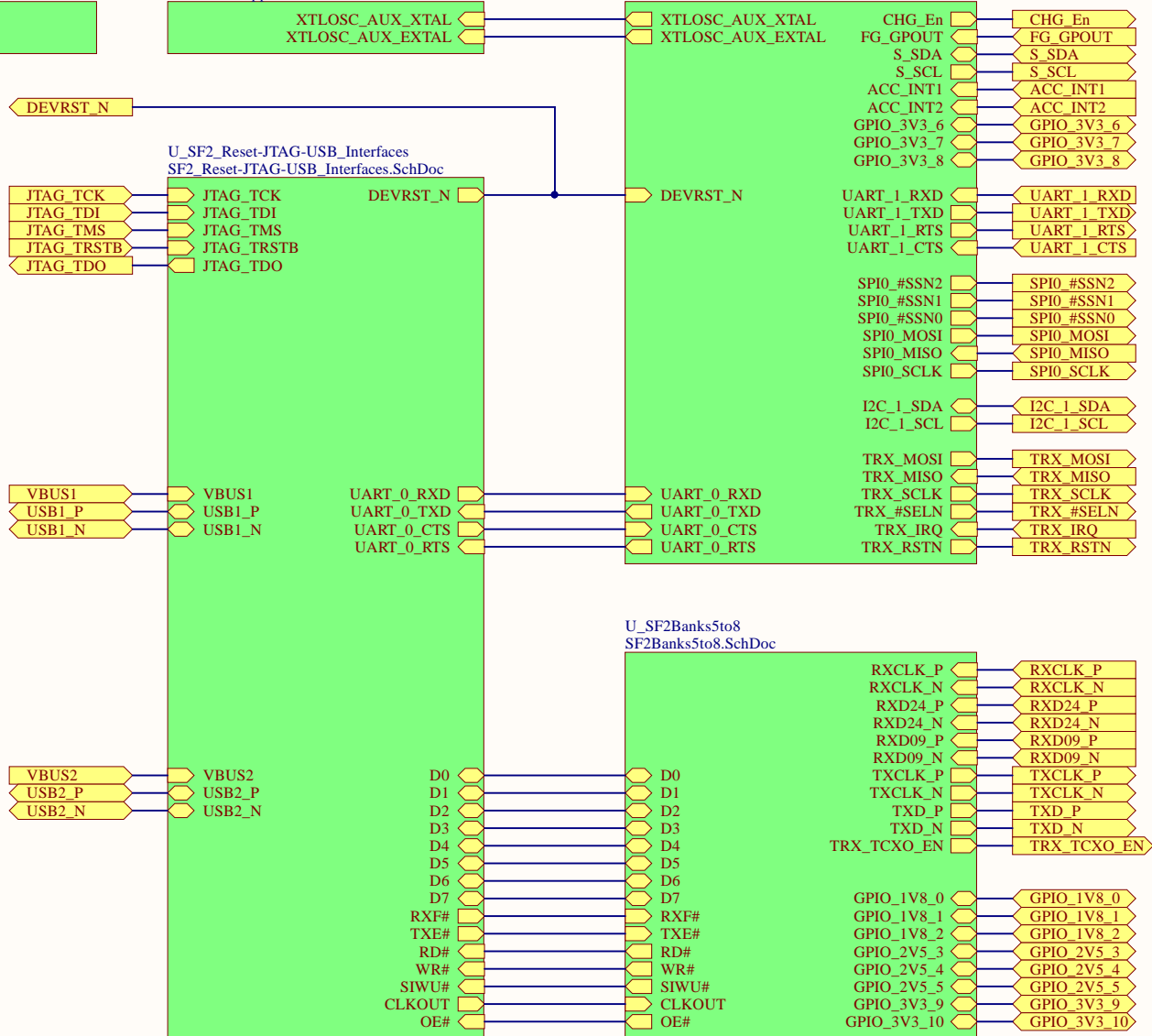
U\_SF2AnalogSupplies  
SF2AnalogSupplies.SchDoc

U\_SF2PowerSupplies  
SF2PowerSupplies.SchDoc

U\_SF2ClockAndBanks013  
SF2ClockAndBanks013.SchDoc

U\_SF2\_Reset-JTAG-USB\_Interfaces  
SF2\_Reset-JTAG-USB\_Interfaces.SchDoc

U\_SF2Banks5to8  
SF2Banks5to8.SchDoc



Title: **SmartFusion2**

Engineers: Ramiro Utrilla and José Martín

Revision: v1r0

Date: 22/10/2019 Time: 11:31:36

Sheet: 7 of 14

File: D:\Repositorio\migou-platform\MIGOU\Schematics\SF2.SchDoc

**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain

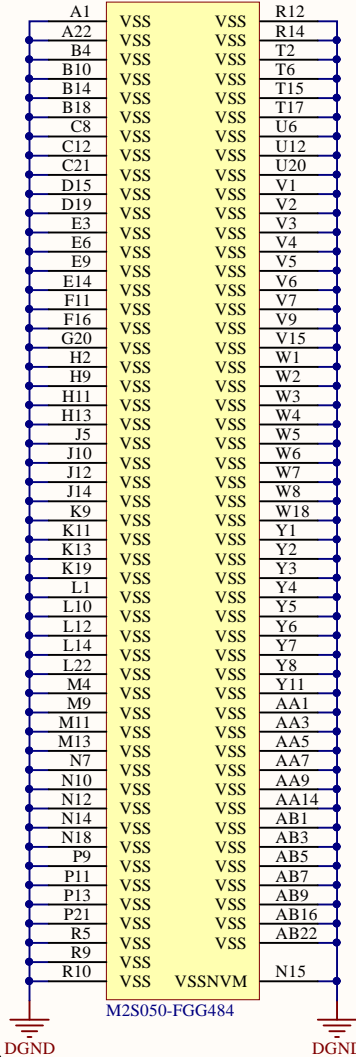




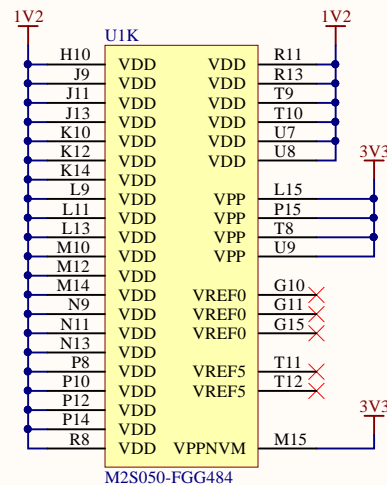
# SF2 POWER SUPPLIES

## GROUNDING

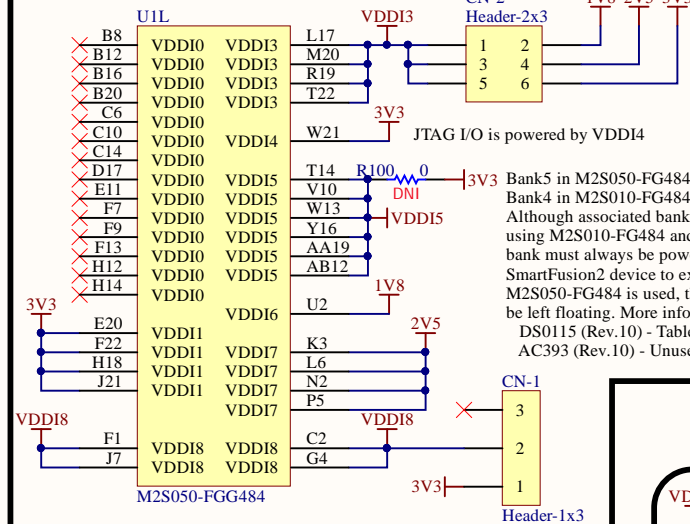
U1M



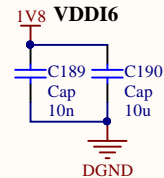
## MAIN POWER SUPPLIES



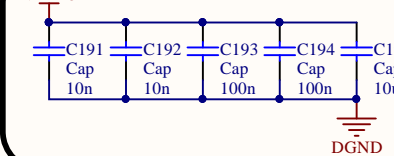
## I/O BANK SUPPLY



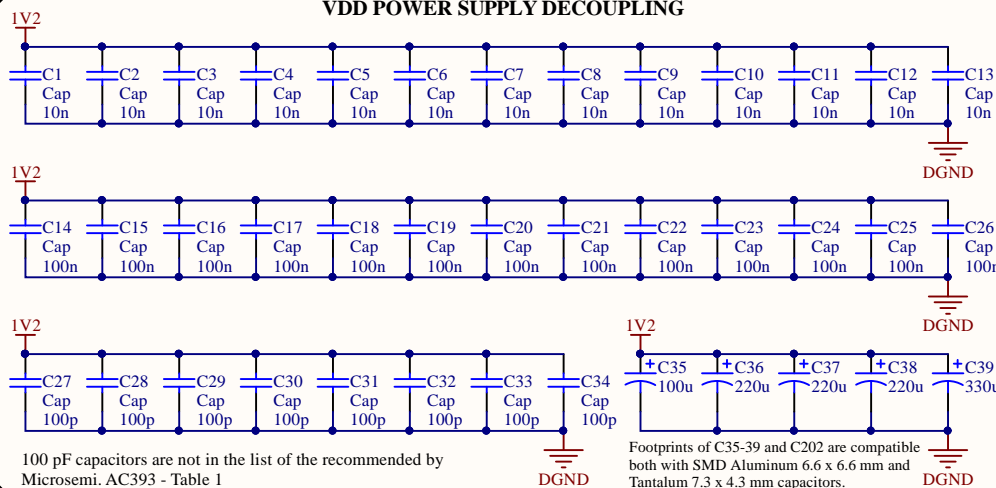
There are three power supply options for the AT86RF215 transceiver (VDD\_TRX). The I/O Bank 3 must have the same power supply voltage, as the communication between the SmartFusion2 and the transceiver is done through the SPI\_1, which is located in that bank. It should be noted that the SPI\_0 and the rest of I/O ports of the bank will operate also : this voltage.



## VDDI8



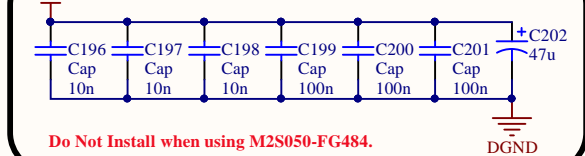
## VDD POWER SUPPLY DECOUPLING



100 pF capacitors are not in the list of the recommended by Microsemi. AC393 - Table 1

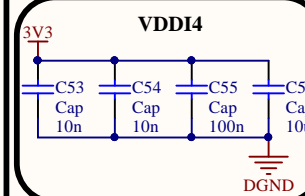
Footprints of C35-39 and C202 are compatible both with SMD Aluminum 6.6 x 6.6 mm and Tantalum 7.3 x 4.3 mm capacitors.

## VDDI5

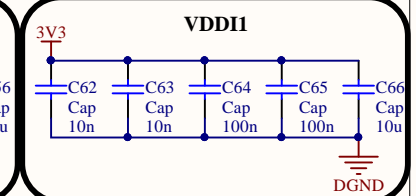


Do Not Install when using M2S050-FG484.

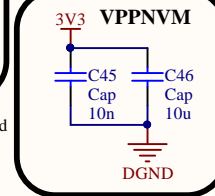
## VDDI4



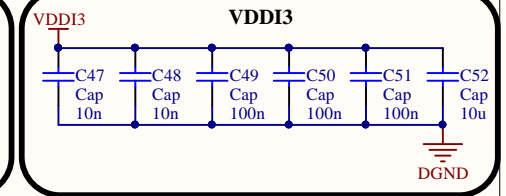
## VDDI1



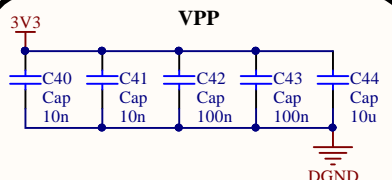
## VPPNVM



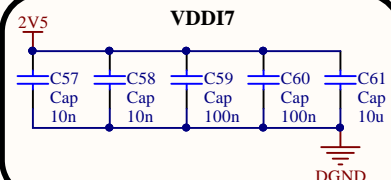
## VDDI3



## VPP



## VDDI7



More info: AC393-Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FGAs.

## Title: SF2 POWER SUPPLIES

Engineers: Ramiro Utrilla and José Martín

Revision: v1r0

Date: 22/10/2019 Time: 11:31:37

Sheet: 8 of 14

File: D:\Repositorio\migou-platform\MIGOU\Schematics\SF2PowerSupplies.SchDoc

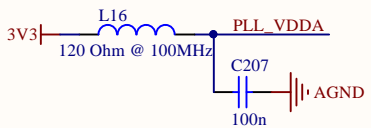
B105 Electronic Systems Lab  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain





# SF2 ANALOG SUPPLIES

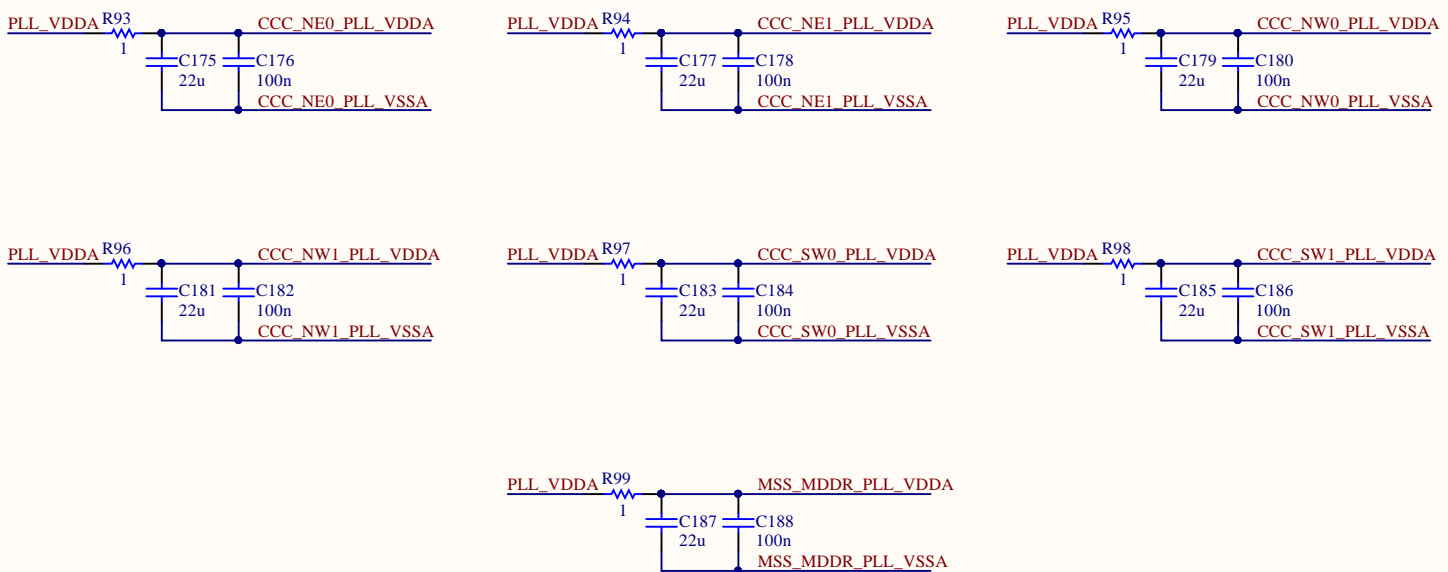
If the associated PLL is used as a clock multiplier, these supplies must be connected over the RC filter circuitry between the common PLL supply and the corresponding on-board PLL return path. If the PLL is unused or used as a clock divider, these supplies can be connected directly to either 2.5V or 3.3V without filter circuitry.



U1J			
CCC_NE0_PLL_VDDA	H15	CCC_NE0_PLL_VDDA	CCC_NE0_PLL_VSSA
CCC_NE1_PLL_VDDA	J17	CCC_NE1_PLL_VDDA	CCC_NE1_PLL_VSSA
CCC_NW0_PLL_VDDA	H8	CCC_NW0_PLL_VDDA	CCC_NW0_PLL_VSSA
CCC_NW1_PLL_VDDA	G9	CCC_NW1_PLL_VDDA	CCC_NW1_PLL_VSSA
CCC_SW0_PLL_VDDA	T5	CCC_SW0_PLL_VDDA	CCC_SW0_PLL_VSSA
CCC_SW1_PLL_VDDA	R7	CCC_SW1_PLL_VDDA	CCC_SW1_PLL_VSSA
MSS_MDDR_PLL_VDDA	H16	MSS_MDDR_PLL_VDDA	MSS_MDDR_PLL_VSSA

M2S050-FGG484

VSSA pins provide the internal PLL current return path for VDDAs. These pins must be connected to the corresponding PLL\_VDDA through an RC filter circuit. PLL\_VSSA and VSS are shorted internally in the silicon. Therefore, to filter noise and control long-term jitter, PLL\_VSSA must NOT be connected to an external ground.



# SF2 CLOCK AND BANKS 0, 1 AND 3

U1A M2S050-FGG484

BANK 0

DDRIO49PB0/MDDR\_ADDR14  
DDRIO49NB0/MDDR\_ADDR15  
DDRIO50PB0/MDDR\_ADDR12  
DDRIO50NB0/MDDR\_ADDR13  
DDRIO51PB0/MDDR\_ADDR10  
DDRIO51NB0/MDDR\_ADDR11  
DDRIO52PB0/MDDR\_ADDR8  
DDRIO52NB0/MDDR\_ADDR9  
DDRIO53PB0/MDDR\_ODT  
DDRIO53NB0/MDDR\_ADDR7  
DDRIO54PB0/MDDR\_ADDR5  
DDRIO54NB0/MDDR\_ADDR6  
DDRIO55PB0/MDDR\_ADDR4  
DDRIO55NB0/MDDR\_ADDR4  
DDRIO56PB0/MDDR\_ADDR1  
DDRIO56NB0/MDDR\_ADDR2  
DDRIO57PB0/MDDR\_BA2  
DDRIO57NB0/MDDR\_ADDR0  
DDRIO58PB0/MDDR\_BA0  
DDRIO58NB0/MDDR\_BA1  
DDRIO59PB0/MDDR\_CLK  
DDRIO59NB0/MDDR\_CLK\_N  
DDRIO60PB0/MDDR\_RESET\_N  
DDRIO60NB0/MDDR\_CAS\_N  
DDRIO61PB0/MDDR\_CKE  
DDRIO61NB0/MDDR\_CS\_N  
DDRIO62PB0/MDDR\_RAS\_N  
DDRIO62NB0/MDDR\_WE\_N  
DDRIO66PB0  
DDRIO66NB0  
DDRIO67PB0  
DDRIO67NB0  
DDRIO72PB0  
DDRIO72NB0  
DDRIO74PB0  
DDRIO74NB0  
DDRIO75PB0/CCC\_NE1\_CLKI3/MDDR\_DQ14  
DDRIO75NB0/MDDR\_DQ15  
DDRIO76PB0/GB12/CCC\_NE1\_CLKI2/MDDR\_DQ12  
DDRIO76NB0/MDDR\_DQ13  
DDRIO77PB0/MDDR\_TMATCH\_0\_IN  
DDRIO77NB0/MDDR\_DM\_RDQS1  
DDRIO78PB0/GB8/CCC\_NE0\_CLKI3/MDDR\_DQS1  
DDRIO78NB0/MDDR\_DQS1\_N  
DDRIO79PB0/CCC\_NE0\_CLKI2/MDDR\_DQ10  
DDRIO79NB0/MDDR\_DQ11  
DDRIO80PB0/MDDR\_DQ8  
DDRIO80NB0/MDDR\_DQ9  
DDRIO81PB0/MDDR\_DQ7  
DDRIO81NB0/MDDR\_TMATCH\_0\_OUT  
DDRIO82PB0/MDDR\_DQ5  
DDRIO82NB0/MDDR\_DQ6  
DDRIO83PB0/MDDR\_DM\_RDQS0  
DDRIO83NB0/MDDR\_DQ4  
DDRIO84PB0/MDDR\_DQS0  
DDRIO84NB0/MDDR\_DQS0\_N  
DDRIO85PB0/MDDR\_DQ2  
DDRIO85NB0/MDDR\_DQ3  
DDRIO86PB0/MDDR\_DQ0  
DDRIO86NB0/MDDR\_DQ1  
DDRIO87PB0/CCC\_NW1\_CLKI3/MDDR\_DQ\_ECC1  
DDRIO87NB0/MDDR\_DQ\_ECC0  
DDRIO88PB0  
DDRIO88NB0  
DDRIO89PB0/MDDR\_TMATCH\_ECC\_IN  
DDRIO89NB0/MDDR\_DM\_RDQS\_ECC  
DDRIO90PB0/MDDR\_DQS\_ECC  
DDRIO90NB0/MDDR\_DQS\_ECC\_N  
DDRIO92PB0/MDDR\_TMATCH\_ECC\_OUT  
DDRIO92NB0/CCC\_NW0\_CLKI2

U1B

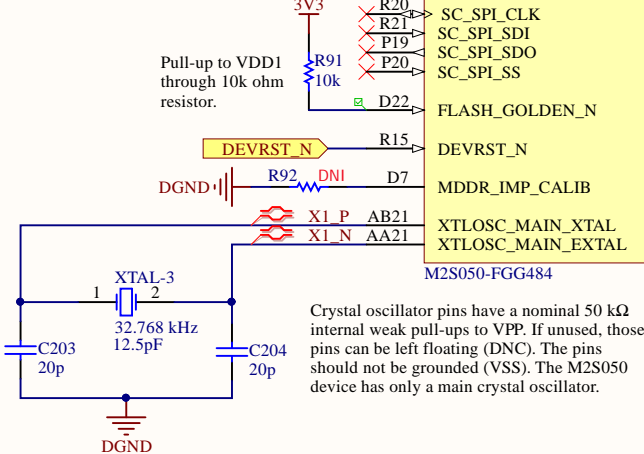
BANK 1

MSIO38PB1/MMUART\_1\_RTS/GPIO\_11\_B  
MSIO38NB1/MMUART\_1\_DTR/GPIO\_12\_B  
MSIO39PB1/CCC\_NE0\_CLKI1/MMUART\_1\_CTS/GPIO\_13\_B  
MSIO39NB1/MMUART\_1\_DSR/GPIO\_14\_B  
MSIO40PB1/CCC\_NE1\_CLKI1/MMUART\_1\_RI/GPIO\_15\_B  
MSIO40NB1/MMUART\_1\_DCD/GPIO\_16\_B  
MSIO41PB1/GB10/VCCC\_SEO\_CLKI  
MSIO41NB1/MMUART\_1\_TXD/GPIO\_24\_B  
MSIO42PB1/GB14/VCCC\_SE1\_CLKI/MMUART\_1\_CLK/GPIO\_25\_B  
MSIO42NB1/MMUART\_1\_RXD/GPIO\_26\_B  
MSIO43PB1/MMUART\_0\_RTS/GPIO\_17\_B  
MSIO43NB1/MMUART\_0\_DTR/GPIO\_18\_B  
MSIO44PB1/MMUART\_0\_CTS/GPIO\_19\_B  
MSIO44NB1/MMUART\_0\_DSR/GPIO\_20\_B  
MSIO45PB1/MMUART\_0\_RI/GPIO\_21\_B  
MSIO45NB1/MMUART\_0\_DCD/GPIO\_22\_B  
MSI46NB1/MMUART\_0\_TXD/GPIO\_27\_B  
MSIO47PB1/MMUART\_0\_RXD/GPIO\_28\_B  
MSIO47NB1/MMUART\_0\_CLK/GPIO\_29\_B  
MSIO48PB1/I2C\_0\_SDA/GPIO\_30\_B  
MSIO48NB1/I2C\_0\_SCL/GPIO\_31\_B

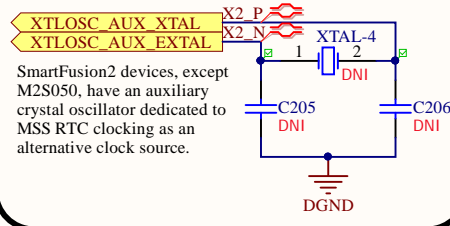
UART\_1\_RTS  
UART\_1\_CTS  
GPIO\_3V3\_6  
UART\_1\_TXD  
GPIO\_3V3\_7  
UART\_1\_RXD  
UART\_0\_RTS  
GPIO\_3V3\_8  
UART\_0\_CTS  
CHG\_En  
ACC\_INT1  
ACC\_INT2  
UART\_0\_TXD  
UART\_0\_RXD  
FG\_GPOUT  
S\_SDA  
S\_SCL

M2S050-FGG484

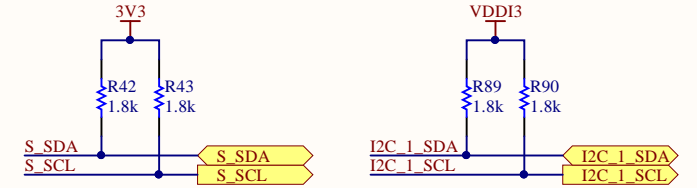
## MAIN CRYSTAL OSCILLATOR



## AUXILIARY CRYSTAL OSCILLATOR



The pins of an unused crystal oscillator can be left floating (DNC) and should not be grounded.



U1C

BANK 3

MSIO0PB3  
MSIO0NB3  
MSIO1PB3  
MSIO1NB3  
MSIO2PB3  
MSIO2NB3  
MSIO3PB3  
MSIO3NB3  
MSIO4PB3  
MSIO4NB3  
MSIO5PB3  
MSIO5NB3  
MSIO6PB3  
MSIO6NB3  
MSIO7PB3  
MSIO7NB3/CAN\_TX/GPIO\_2\_A  
MSIO8PB3/CAN\_RX/GPIO\_3\_A  
MSIO8NB3/CAN\_TX\_EN\_N/GPIO\_4\_A  
MSIO11PB3/CCC\_NE0\_CLKI0/I2C\_1\_SDA/GPIO\_0\_A  
MSIO11NB3/CCC\_NE1\_CLKI0/I2C\_1\_SCL/GPIO\_1\_A  
MSIO12PB3/SPI\_0\_CLK  
MSIO12NB3/SPI\_0\_SDI/GPIO\_5\_A  
MSIO13PB3/SPI\_0\_SDO/GPIO\_6\_A  
MSIO13NB3/SPI\_0\_SS0/GPIO\_7\_A  
MSIO14PB3/SPI\_0\_SS4/GPIO\_19\_A  
MSIO14NB3/SPI\_0\_SS5/GPIO\_20\_A  
MSIO15PB3/SPI\_0\_SS6/GPIO\_21\_A  
MSIO15NB3/SPI\_0\_SS7/GPIO\_22\_A  
MSIO16PB3/SPI\_1\_CLK  
MSIO16NB3/SPI\_1\_SDI/GPIO\_11\_A  
MSIO17PB3/SPI\_1\_SDO/GPIO\_12\_A  
MSIO17NB3/SPI\_1\_SS0/GPIO\_13\_A  
MSIO18PB3/SPI\_1\_SS4/GPIO\_17\_A  
MSIO18NB3/SPI\_1\_SS5/GPIO\_18\_A  
MSIO19PB3/SPI\_1\_SS6/GPIO\_23\_A  
MSIO19NB3/SPI\_1\_SS7/GPIO\_24\_A  
MSIO20PB3/GB9/VCCC\_SEO\_CLKI/GPIO\_25\_A  
MSIO20NB3/GB13/VCCC\_SE1\_CLKI/GPIO\_26\_A  
MSIO22PB3/SPI\_0\_SS1/GPIO\_8\_A  
MSIO22NB3/SPI\_0\_SS2/GPIO\_9\_A  
MSIO23PB3/SPI\_0\_SS3/GPIO\_10\_A  
MSIO23NB3/SPI\_1\_SS1/GPIO\_14\_A  
MSIO24PB3/SPI\_1\_SS2/GPIO\_15\_A  
MSIO24NB3/SPI\_1\_SS3/GPIO\_16\_A

I2C\_1\_SDA  
I2C\_1\_SCL  
SPIO\_SCLCK  
SPIO\_MISO  
SPIO\_MOSI  
SPIO\_SSNO  
TRX\_SCLCK  
TRX\_MISO  
TRX\_SELN  
TRX\_IRQ  
TRX\_RSTN  
SPIO\_SSNN1  
SPIO\_SSNN2

M2S050-FGG484

Title: **SF2 CLOCK AND BANKS 0, 1 AND 3**

Engineers: Ramiro Utrilla and José Martín

Revision: v1r0

Date: 22/10/2019 Time: 11:31:40

Sheet: 10 of 14

File: D:\Repositorio\migou-platform\MIGOU\Schematics\SF2ClockAndBanks013.SchDoc

B105 Electronic Systems Lab  
ETSII Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain



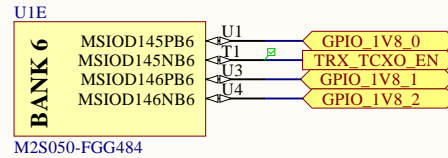
# SF2 BANKS 5 TO 8

## NOT USED

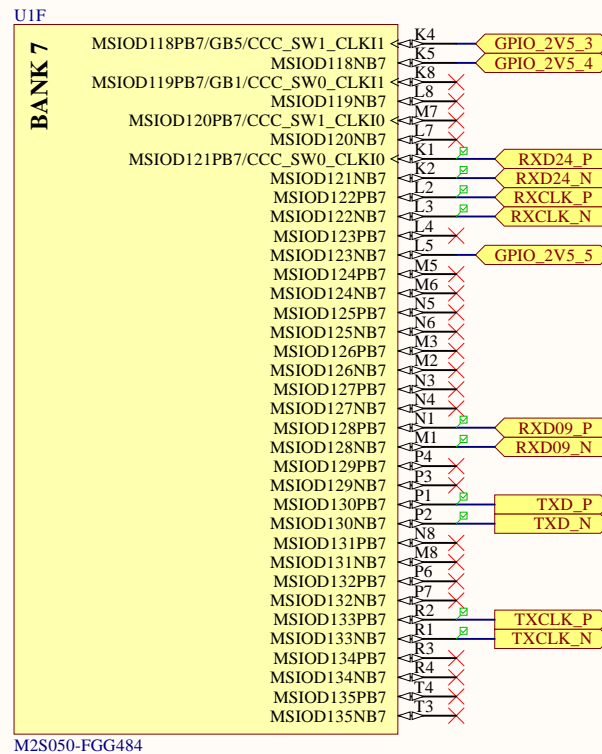
UID	M2S050-FGG484
<b>BANK 5</b>	<div> <div>W9</div> <div>Y9</div> <div>AA10</div> <div>AB10</div> <div>W10</div> <div>Y10</div> <div>AA11</div> <div>AB11</div> <div>U10</div> <div>U11</div> <div>V11</div> <div>AA12</div> <div>Y12</div> <div>W12</div> <div>V12</div> <div>AB13</div> <div>AB14</div> <div>AA13</div> <div>Y13</div> <div>AB15</div> <div>AA15</div> <div>U13</div> <div>T13</div> <div>AA16</div> <div>AA17</div> <div>Y14</div> <div>W14</div> <div>V13</div> <div>V14</div> <div>W15</div> <div>W16</div> <div>AA18</div> <div>U14</div> <div>U15</div> <div>AB18</div> <div>AB19</div> <div>Y18</div> <div>Y19</div> <div>Y17</div> <div>W17</div> <div>W16</div> <div>V16</div> <div>U16</div> <div>T16</div> <div>Y20</div> <div>W19</div> <div>V17</div> <div>U17</div> <div>V18</div> <div>U18</div> </div> <div> <div>DDRIO148PB5/PROBE_A</div> <div>DDRIO148NB5/PROBE_B</div> <div>DDRIO149PB5</div> <div>DDRIO149NB5</div> <div>DDRIO151PB5</div> <div>DDRIO151NB5</div> <div>DDRIO152PB5/GB3/CCC_SW0_CLKI3</div> <div>DDRIO152NB5/GB7/CCC_SW1_CLKI2</div> <div>DDRIO154PB5</div> <div>DDRIO154NB5</div> <div>DDRIO156PB5</div> <div>DDRIO156NB5</div> <div>DDRIO157PB5</div> <div>DDRIO157NB5</div> <div>DDRIO159PB5/CCC_SW1_CLKI3</div> <div>DDRIO159NB5</div> <div>DDRIO161PB5/GB11/VCCC_SE0_CLKI</div> <div>DDRIO161NB5</div> <div>DDRIO162PB5</div> <div>DDRIO162NB5</div> <div>DDRIO164PB5/VCCC_SE1_CLKI</div> <div>DDRIO164NB5</div> <div>DDRIO166PB5</div> <div>DDRIO166NB5</div> <div>DDRIO167PB5</div> <div>DDRIO167NB5</div> <div>DDRIO169PB5</div> <div>DDRIO169NB5</div> <div>DDRIO171PB5</div> <div>DDRIO171NB5</div> <div>DDRIO172PB5</div> <div>DDRIO172NB5</div> <div>DDRIO174PB5</div> <div>DDRIO174NB5</div> <div>DDRIO176PB5</div> <div>DDRIO176NB5</div> <div>DDRIO177PB5</div> <div>DDRIO177NB5</div> <div>DDRIO181PB5</div> <div>DDRIO181NB5</div> <div>DDRIO182PB5</div> <div>DDRIO182NB5</div> <div>DDRIO184PB5</div> <div>DDRIO184NB5</div> <div>DDRIO186PB5</div> <div>DDRIO186NB5</div> <div>DDRIO187PB5</div> <div>DDRIO187NB5</div> <div>DDRIO189PB5</div> <div>DDRIO189NB5</div> <div>DDRIO190PB5</div> <div>DDRIO190NB5</div> </div>

Low pinout compatibility between BANK5 (M2S050) and BANK4 (M2S010 and M2S025). Special care should be taken if you decide to use any of these pins in the future.

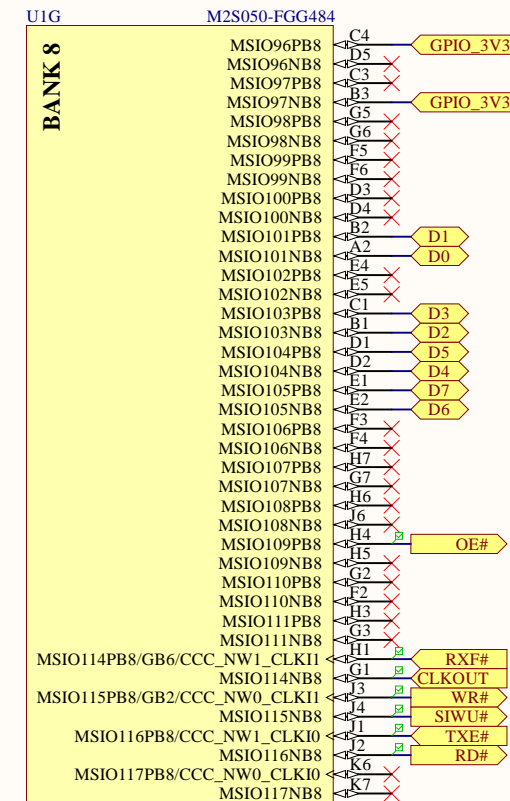
## 1V8 LOGIC



## 2V5 LOGIC



## 3V3 LOGIC



Title: **SF2 BANKS 5 TO 8**

Engineers: Ramiro Utrilla and José Martín

Revision: v1r0

Date: 22/10/2019

Time: 11:31:41

Sheet: 11 of 14

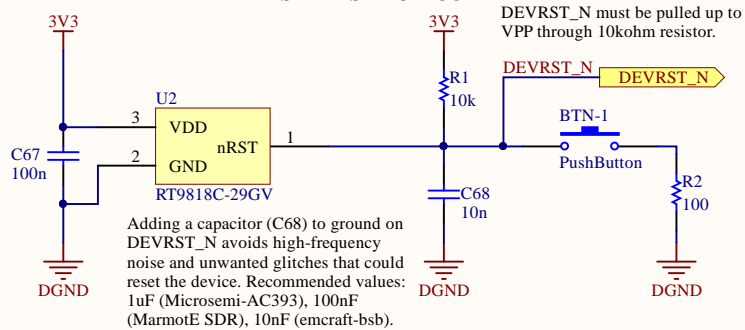
File: D:\Repositorio\migou-platform\MIGOU\Schematics\SF2Banks5to8.SchDoc

**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain

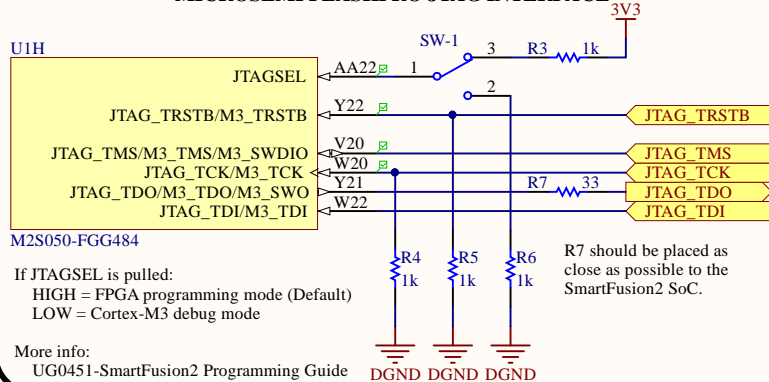


# SF2 RESET, JTAG AND USBs

## SF2 RESET CIRCUIT

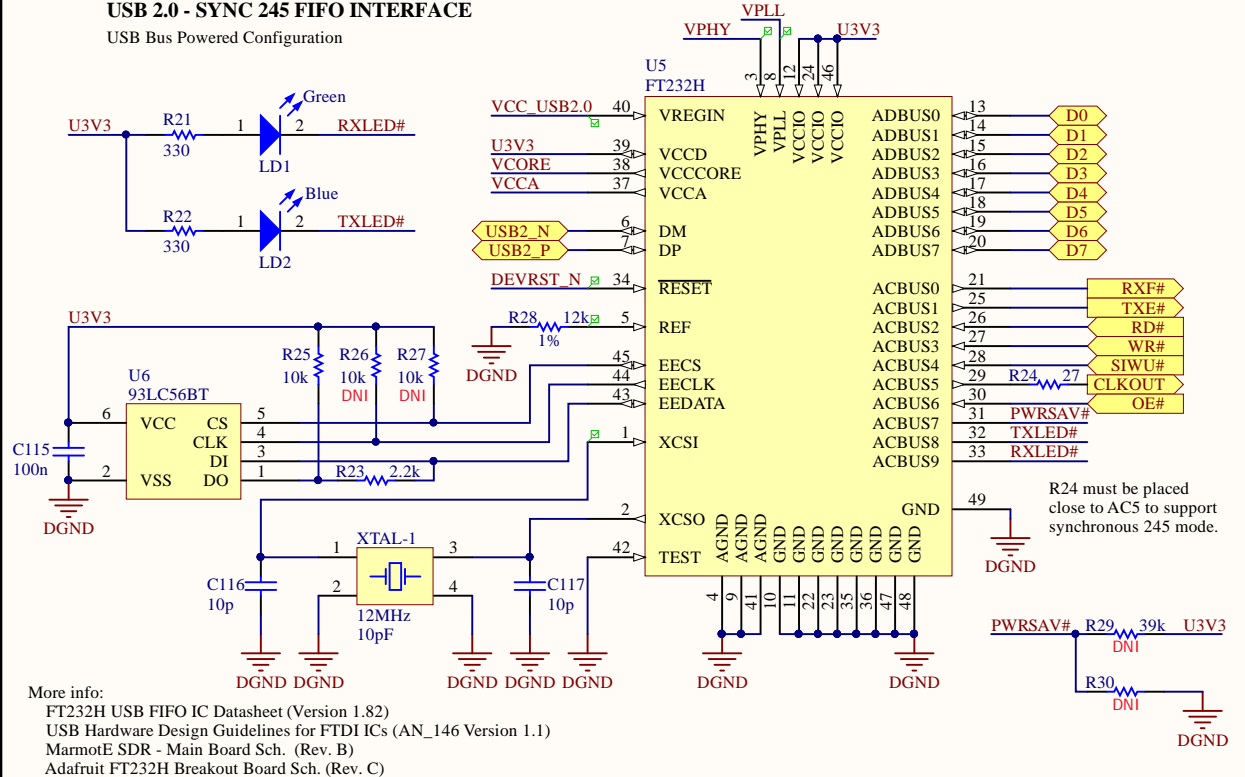


## MICROSEMI FLASHPRO JTAG INTERFACE



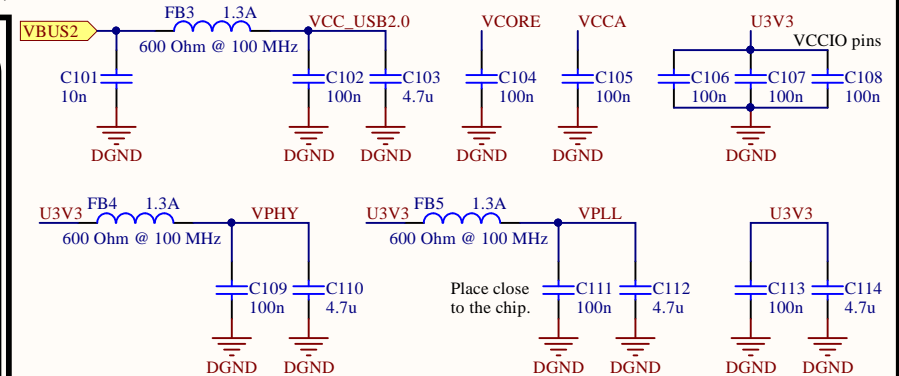
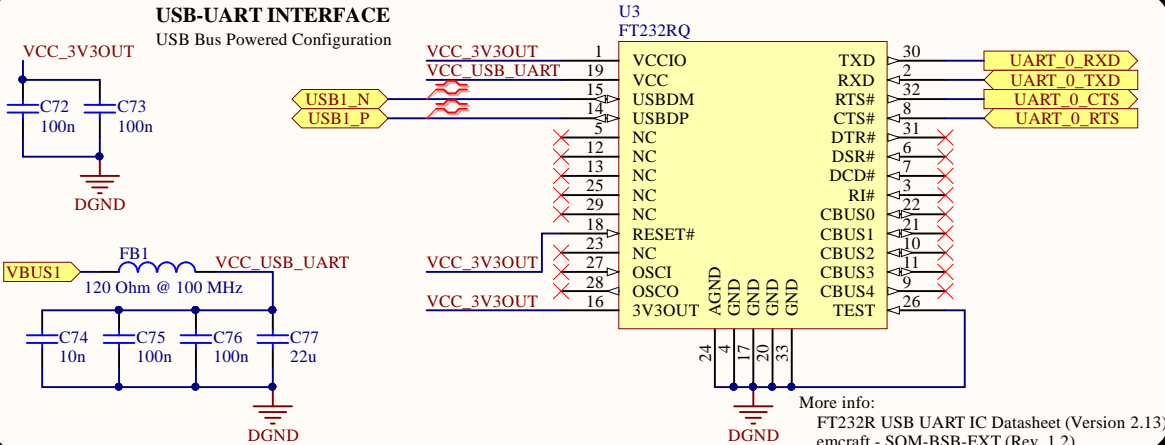
## USB 2.0 - SYNC 245 FIFO INTERFACE

USB Bus Powered Configuration



## USB-UART INTERFACE

USB Bus Powered Configuration



Title: **SF2 RESET, JTAG AND USBs**

Engineers: Ramiro Utrilla and José Martín

Revision: v1r0

Date: 22/10/2019 Time: 11:31:43

Sheet: 12 of 14

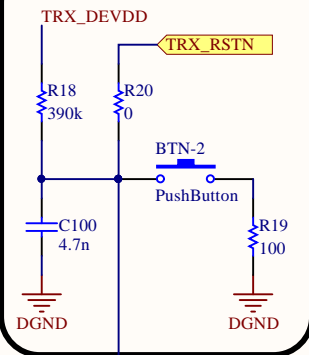
File: D:\Repositorio\migou-platform\MIGOU\Schematics\SF2\_Reset-JTAG-USB\_Interfaces.SchDoc

**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain



# RF FRONT-END

## TRX RESET CIRCUIT



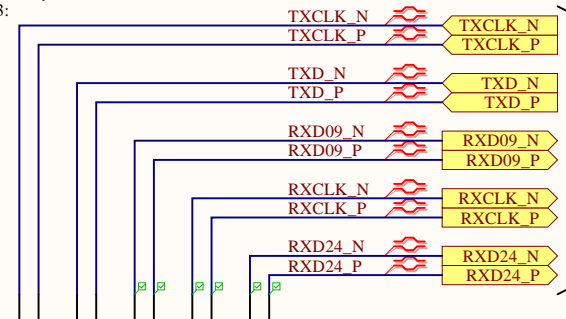
The LVDS signals differential impedance must be 100 ohm. On a 4 layer board with 0.195 mm between outer and inner layers and with substrate dielectric 4.3:

- Trace Thickness: 17.5 um
- Trace Width 0.22 mm
- Trace spacing: 0.15 mm

Result: Zdiff: 100.646 ohm

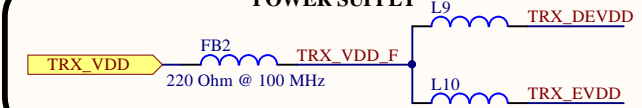
## TRX SPI INTERFACE

TRX\_MISO  
TRX\_MOSI  
TRX\_SELN  
TRX\_SCLK

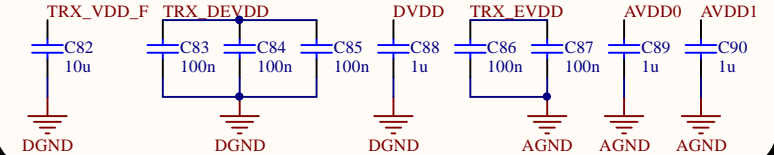


lvds signals

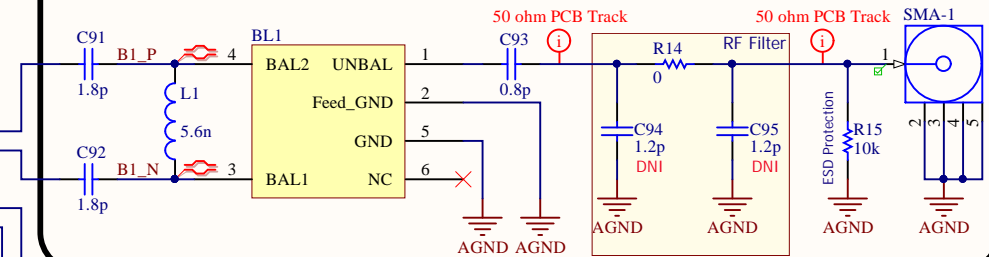
## POWER SUPPLY



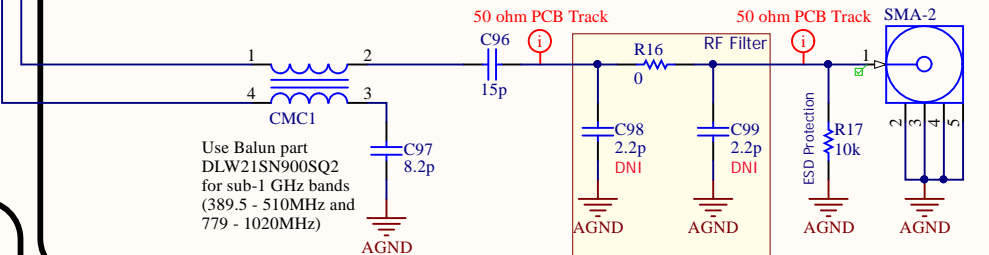
## DECOUPLING CAPACITORS



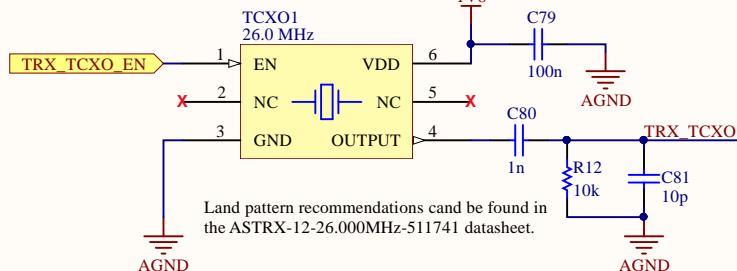
## 2.4 GHz BAND



## SUB-1 GHz BAND

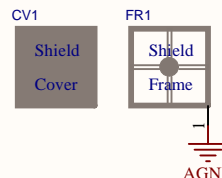


## TRX CLOCK CIRCUIT



Land pattern recommendations can be found in the ASTRX-12-26.000MHz-511741 datasheet.

## RF SHIELDING



Title: **RF FRONT-END**

Engineers: Ramiro Utrilla and José Martín

Revision: v1r0

Date: 22/10/2019 Time: 11:31:44

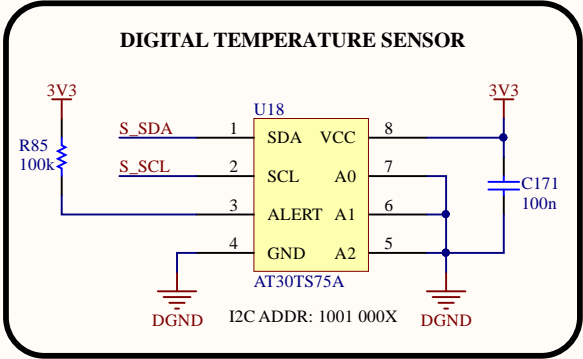
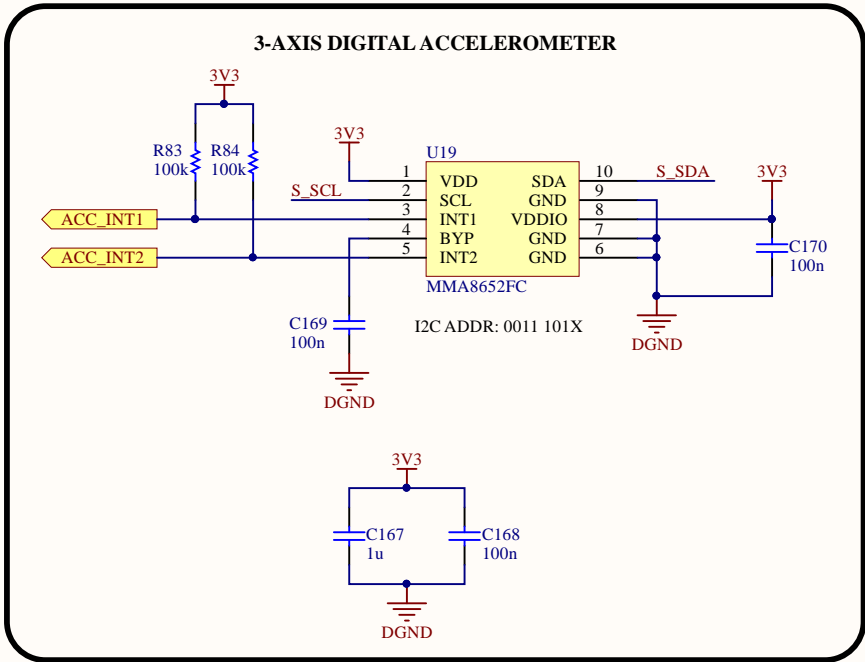
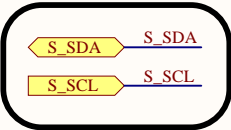
Sheet: 13 of 14

File: D:\Repositorio\migou-platform\MIGOU\Schematics\RF\_Front-End.SchDoc

**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain



# SENSORS



Title: **SENSORS**

Engineers: Ramiro Utrilla and José Martín

Revision: v1r0

Date: 22/10/2019

Time: 11:31:45

Sheet: 14 of 14

File: D:\Repositorio\migou-platform\MIGOU\Schematics\Sensors.SchDoc

**B105 Electronic Systems Lab**  
ETSI Telecomunicación, B-105  
Universidad Politécnica de Madrid  
Avda. Complutense, 30  
28040 Madrid - Spain

